AMENDMENTS TO THE CLAIMS

Claim 1. (currently amended): A memory device comprising:

a memory array comprising at least a first storage area and a second storage area, said first storage area including at least a first block and said second storage area including at least a second block, ~~each of said at least first and second blocks~~ each of said first and second blocks including a plurality of sectors;

a buffer;

a control circuit coupled to the memory array and the buffer for accepting external commands and for reading, writing, and erasing portions of said memory array;[[,]] ~~said control circuit, responsive to a data transfer command, copies at least one sector from said first storage area to at least one sector in said second storage area without transferring the contents of said at least one sector to an external bus.~~

wherein said control circuit is responsive to a data transfer command, said data transfer command including a source address of a first sector in said first block, a destination address of a second sector in said second block, and a parameter specifying an amount of data, to copy the amount of data specified from sectors in said first block starting with said first sector and to sectors in said second block starting with said second sector, without transferring any content on an external bus.

Claim 2. (cancel):

Claim 3. (original): The memory device of claim 1, wherein said at least one sector is a plurality of sectors.

Claims 4-5. (cancel):

Claim 6. (original): The memory device of claim 1, wherein said memory is a non-volatile memory.

Claim 7. (original): The memory device of claim 6, wherein said memory is a flash memory.

Claim 8. (original): The memory device of claim 1, wherein each sector of said second block has a size which is at least as large as each corresponding sector of said first block.

Claim 9. (original): The memory device of claim 8, wherein said second block has at least as many sectors as said first block.

Claim 10. (original): The memory device of claim 9, wherein said first and second blocks have identical number of sectors.

Claim 11. (original): The memory device of claim 10, wherein each sector is a same size.

Claim 12. (original): The memory device of claim 1, wherein said control circuit causes said at least one sector to be first copied from said first block to the buffer and subsequently copied from the buffer to said second block.

Claims 13-14. (cancel):

Claim 15. (currently amended): A ~~The~~ memory device ~~of claim 13,~~ comprising:

a memory array comprising at least a first storage area and a second storage area, said first storage area including at least a first block and said second storage area including at least a second block, each of said first and second blocks including a plurality of sectors;

a buffer;

a control circuit coupled to the memory array and the buffer for accepting external commands and for reading, writing, and erasing portions of said memory array;

wherein said control circuit is responsive to a data transfer command, said data transfer command including a source address of a first sector in said first block, a destination address of a second sector in said second block, and a count parameter specifying a number of additional sectors, to copy contents sectors in said first block starting with said first sector and continuing for said additional sectors to sectors in said second block starting with said second sector, without transferring any content on an external bus.

~~wherein said data transfer command includes a count parameter specifying a number of additional sectors starting from the source address which are copied to a corresponding number of sectors starting at the destination address.~~

Claim 16. (original): The memory device of claim 1, wherein said control circuit,

responsive to an erase command issued after the data transfer command, erases each sector of said first block; and

responsive to a second data transfer command issued after the erase command, copies the at least one sector from said second block to said first block.

Claim 17. (original): The memory device of claim 1, wherein said control circuit further comprises:

a logic circuit for decoding commands; and

a state machine for executing decoded commands.

Claim 18. (currently amended): A memory system comprising:

an external bus;

a controller coupled to said external bus;

a memory, coupled to said controller[[,]] via said external bus, wherein said memory further comprises:

a memory array comprising at least a first storage area and a second storage area, said first storage area including at least a first block and said second storage area including at least a second block, ~~each of said at least first and second blocks~~ each of said first and second blocks including a plurality of sectors;

a buffer;

a control circuit coupled to the memory array and the buffer for accepting external commands and for reading, writing, and erasing portions of said memory array;[[,]]

wherein said control circuit[[,]] is responsive to a data transfer command, said data transfer command including a source address of a first sector in said first block, a destination address of a second sector in said second block, and a length parameter specifying a total number of sectors starting from the source address to be copied to the destination address, to copy contents of sectors in said first block starting with said first sector and continuing for a number of sectors so that a total number of sectors transferred is equal to said length parameter, to sectors in said second block starting with said second sector, ~~copies at least one sector from said first storage area to at least one sector in said second storage area~~ without transferring any ~~the~~ content[[s]] ~~of said at least one sector~~ to said ~~an~~ external bus.

Claim 19. (cancel):

Claim 20. (original): The memory system of claim 18, wherein said at least one sector is a plurality of sectors.

Claims 21-22. (cancel):

Claim 23. (original): The memory system of claim 18, wherein said memory is a non-volatile memory.

Claim 24. (original): The memory system of claim 23, wherein said memory is a flash memory.

Claim 25. (original): The memory system of claim 18, wherein each sector of said second block has a size which is at least as large as each corresponding sector of said first block.

Claim 26. (original): The memory system of claim 25, wherein said second block has at least as many sectors as said first block.

Claim 27. (original): The memory system of claim 26, wherein said first and second blocks have identical number of sectors.

Claim 28. (original): The memory system of claim 27, wherein each sector is a same size.

Claim 29. (original): The memory system of claim 18, wherein said control circuit causes said at least one sector to be first copied from said first block to the buffer and subsequently copied from the buffer to said second block.

Claims 30-31. (cancel):

Claim 32. (currently amended): A ~~The~~ memory system ~~of claim 30,~~ comprising:

an external bus;

a controller coupled to said external bus;

a memory, coupled to said controller via said external bus, wherein said memory further comprises:

a memory array comprising at least a first storage area and a second storage area, said first storage area including at least a first block and said second storage area including at least a second block, each of said first and second blocks including a plurality of sectors;

a buffer;

a control circuit coupled to the memory array and the buffer for accepting external commands and for reading, writing, and erasing portions of said memory array;

wherein said control circuit is responsive to a data transfer command, said data transfer command including a source address of a first sector in said first block, a destination address of a second sector in said second block, and a count parameter specifying a number of additional sectors, to copy contents sectors in said first block starting with said first sector and continuing for said additional sectors to sectors in said second block starting with said second sector, without transferring any content on said external bus.

~~wherein said data transfer command includes a count parameter specifying a number of additional sectors starting from the source address which are copied to a corresponding number of sectors starting at the destination address.~~

Claim 33. (original): The memory system of claim 18, wherein said control circuit,

responsive to an erase command issued after the data transfer command, erases each sector of said first block; and

responsive to a second data transfer command issued after the erase command, copies the at least one sector from said second block to said first block.

Claim 34. (currently amended): The memory system of claim 18, wherein said control circuit further comprises:

a logic circuit for decoding commands; and

a state machine for ~~decoded~~ executing decoded commands.

Claim 35. (currently amended): A method of transferring data in a memory device comprising at least a first block and a second block,[[s]] each of said first and second block comprising a plurality of sectors, ~~of storage locations,~~ the method comprising:

(a) receiving a data transfer command, said data transfer command specifying a first sector in said first block, a second sector in said second block, and a parameter specifying an amount of data to be copied from said first block to said second block;

(b) ~~(a)~~ copying data starting from the [[a]] first sector ~~in the first block of said memory device~~ to a buffer of said memory device;

(c) ~~(b)~~ starting with said second sector, copying data from the buffer to ~~a second sector in~~ the second block of said memory device;[[.]] and

(d) performing steps (b) and (c) repeatedly until the amount of data specified by the parameter has been copied from said first block to said second block.

Claim 36. (original): The method of claim 35, wherein said memory device is non-volatile.

Claim 37. (original): The method of claim 36, wherein said memory device is a flash memory.

Claim 38. (original): The method of claim 35, wherein each sector of said second block has a size which is at least as large as each corresponding sector of said first block.

Claim 39. (original): The method of claim 35, wherein said second block has at least as many sectors as said first block.

Claim 40. (original): The method of claim 35, wherein said first and second blocks have identical number of sectors.

Claim 41. (original): The method of claim 40, wherein each sector is a same size.

Claim 42. (currently amended): The method of claim 35, wherein said parameter is a count value specifying a total number of sectors to transfer from said first block to said second block. ~~further comprising the steps of:~~

~~(c) receiving a count value from an the external bus interface; and~~

~~(d) performing steps (a) and (b) repeatedly until a number of sectors adjacent to and after said first sector has been copied to corresponding sectors adjacent to and after said second sector;~~

~~wherein said number is equal to the count value.~~

Claim 43. (currently amended): The method of claim 35, wherein said parameter is a length value specifying a number of additional sectors to transfer after said first sector has been transferred to said second block. ~~further:~~

~~(c) receiving a length value from the external bus interface;~~

~~(d) performing steps (a) and (b) repeatedly until a number of sectors beginning with and adjacent to said first sector has been copied to a corresponding number of sectors beginning with and adjacent to said second sector;~~

~~wherein said number is equal to the length value.~~

Claim 44. (original): The method of claim 35, further comprising:

(e) ~~(c)~~ erasing said first block;

(f) ~~(d)~~ copying data from the second sector to said buffer; and

(g) ~~(e)~~ copying data from said buffer to said first sector.

Claim 45-47. (cancel):

Claim 48. (currently amended): A processor system comprising:

a processor;

a memory controller coupled to said processor;

a memory coupled to said controller, wherein said memory further comprises:

a memory array comprising at least a first storage area and a second storage area, said first storage area including at least a first block and said second storage area including at least a second block, ~~each of said at least first and second blocks~~ each of said first and second blocks including a plurality of sectors;

a buffer;

a control circuit coupled to the memory array and the buffer for accepting external commands and for reading, writing, and erasing portions of said memory array;[[,]]

wherein said control circuit[[,]] is responsive to a data transfer command, said data transfer command including a source address of a first sector in said first block, a destination address of a second sector in said second block, and a length parameter specifying a total number of sectors starting from the source address to be copied to the destination address, to copy contents of sectors in said first block starting with said first sector and continuing for a number of sectors so that a total number of sectors transferred is equal to said length parameter, to sectors in said second block starting with said second sector, ~~copies at least one sector from said first storage area to at least one sector in said second storage area~~ without transferring any ~~the~~ content[[s]] ~~of said at least one sector~~ to an external bus.

Claim 49. (cancel):

Claim 50. (currently amended): The processor system ~~memory device~~ of claim 48, wherein said at least one sector is a plurality of sectors.

Claims 51-52. (cancel):

Claim 53. (currently amended): The processor system ~~memory device~~ of claim 48, wherein said memory is a non-volatile memory.

Claim 54. (currently amended): The processor system ~~memory device~~ of claim 53, wherein said memory is a flash memory.

Claim 55. (currently amended): The processor system ~~memory device~~ of claim 48, wherein each sector of said second block has a size which is at least as large as each corresponding sector of said first block.

Claim 56. (currently amended): The processor system ~~memory device~~ of claim 55, wherein said second block has at least as many sectors as said first block.

Claim 57. (currently amended): The processor system ~~memory device~~ of claim 56, wherein said first and second blocks have identical number of sectors.

Claim 58. (currently amended): The processor system ~~memory device~~ of claim 57, wherein each sector is a same size.

Claim 59. (currently amended): The processor system ~~memory device~~ of claim 48, wherein said control circuit causes said at least one sector to be first copied from said first block to the buffer and subsequently copied from the buffer to said second block.

Claims 60-61. (cancel):

Claim 62. (currently amended): A ~~The~~ processor system ~~memory device of claim 60,~~ comprising:

a processor;

a memory controller coupled to said processor;

a memory coupled to said controller, wherein said memory further comprises:

a memory array comprising at least a first storage area and a second storage area, said first storage area including at least a first block and said second storage area

including at least a second block, each of said first and second blocks including a plurality of sectors;

a buffer;

a control circuit coupled to the memory array and the buffer for accepting external commands and for reading, writing, and erasing portions of said memory array;

wherein said control circuit is responsive to a data transfer command, said data transfer command including a source address of a first sector in said first block, a destination address of a second sector in said second block, and a count parameter specifying a number of additional sectors, to copy contents sectors in said first block starting with said first sector and continuing for said additional sectors to sectors in said second block starting with said second sector, without transferring any content on an external bus.

Claim 63. (currently amended): The processor system ~~memory device~~ of claim 48, wherein said control circuit,

responsive to an erase command issued after the data transfer command, erases each sector of said first block; and

responsive to a second data transfer command issued after the erase command, copies the at least one sector from said second block to said first block.

Claim 64. (currently amended): The processor system ~~memory device~~ of claim 48, wherein said control circuit further comprises:

a logic circuit for decoding commands; and

a state machine for executing decoded commands.